

Technologies for Optical Packet Switching

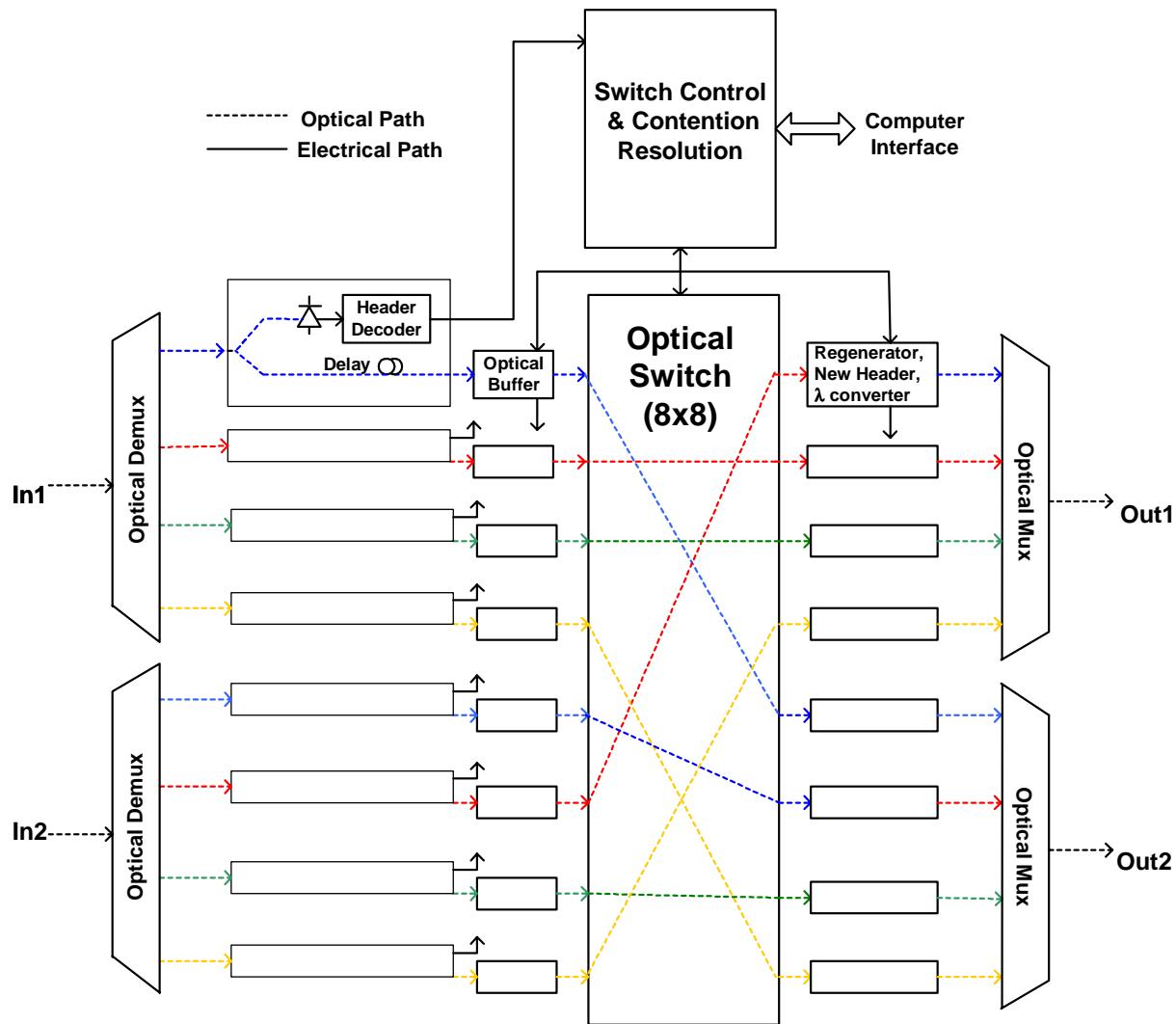
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A Typical Optical Packet Router



Key Components

Photonic Devices

- Switch fabric
- Regenerator
- Delay & buffer
- λ converter
- Header swap
- Source & detector

Electrical ICs

- Mux, driver, Demux
- TIA, LimAmp, CDR
- VCO, mixer,
- Header decoder, FPGA
- Switch control/driver
- New label generation

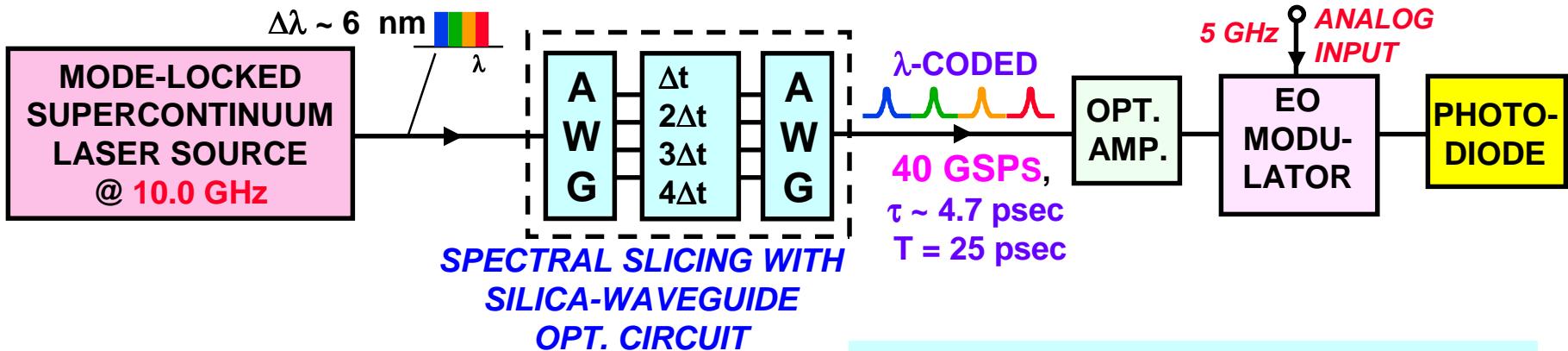
Integration

- Chip scale O-E
- MCM, PCB
- Computer interface

Software

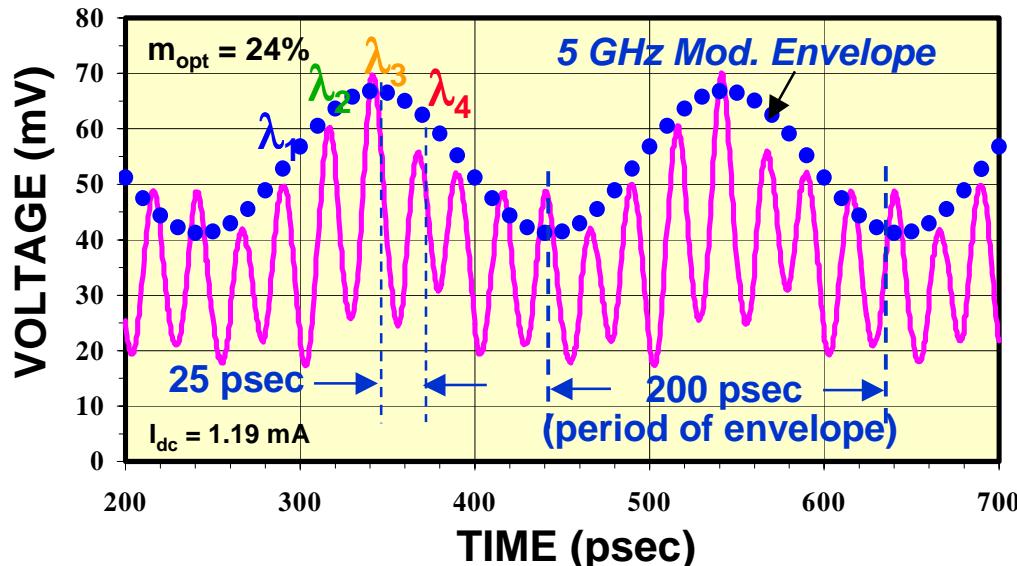
- IP and λ routing
- Network architecture
- Protocols

Photonic Technologies for 160 Gb/s Optical Packet Switching



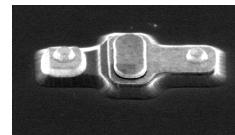
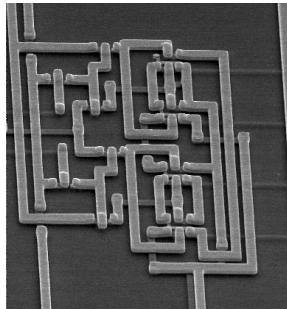
- PICOSECOND TECHNOLOGY
 - Low Jitter (15 fs) ML Laser
- SILICA WAVEGUIDE PLC
 - Header Opt. Correlator
- HIGH SPEED InP OEIC FOR psec SWITCHES AND DRIVER ELECTRONICS
- 3R REGENERATION

40 GHz PHOTONIC SAMPLING OBSERVED WITH 50 GHz SAMPLING SCOPE:



Microelectronics for Optical Packet Switching

- InP HBT technologies

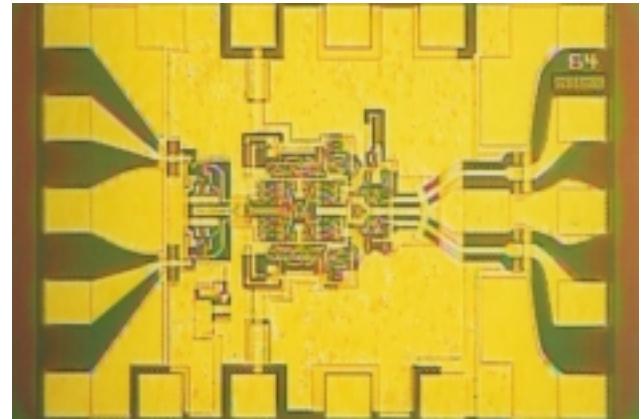


$f_t, f_{max} = 180 \text{ GHz}$
 $1 \times 3 \mu\text{m}^2$

$2 \mu\text{m}$ line/spacing

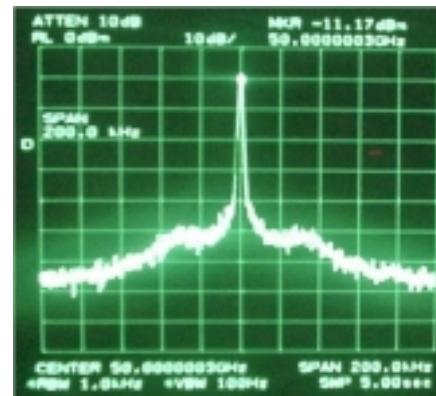
DARPA-funded sub-micron InP HBT technology (TFAST) or ABCS technology in longer term

- High-speed ICs and MMICs



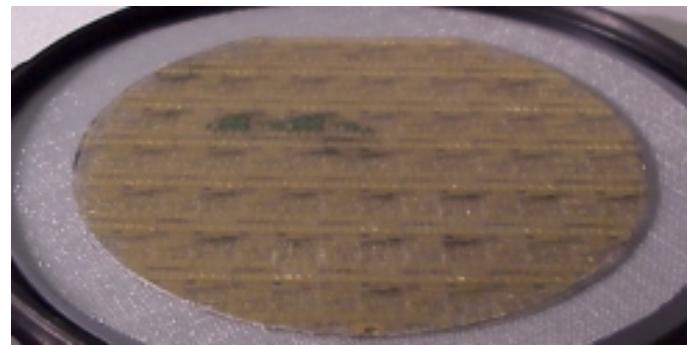
100GHz frequency divider

Metric (unit)	Current	TFAST Phase 1A Milestone	TFAST Goal
Emitter width (μm)	1.0	0.25	0.15
f_t/f_{max} (GHz)	180/180	350/400	500/500
J (kA/cm^2) @ $V_{ce} < 1.5\text{V}$	200	600	1000
Flip-flop speed (GHz) @ < 30mW P_{diss}	75	150	200
Transistor Count		1,000	>20,000

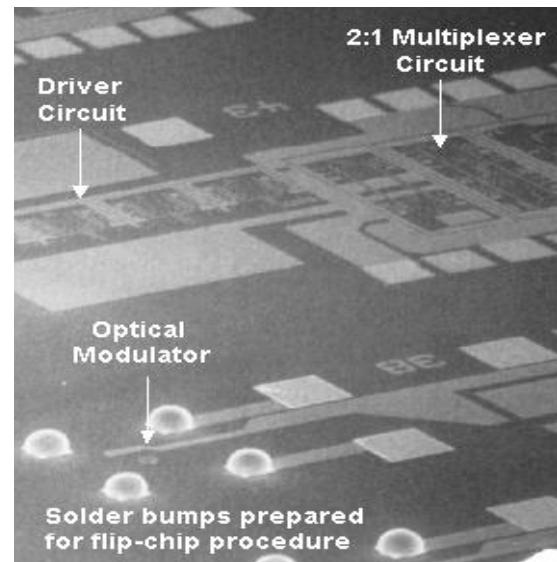


Integration Technologies

- Opto-electronic integration
 - Heterogeneous Integration using wafer bonding.
 - Capable of integrating dissimilar technologies.
 - Quasi-monolithic integration
 - Demonstrated integration of 1 μm emitter InP HBT ICs and Opto-electronic components with >35 GHz BW.
 - Chip scale packaging
- Conventional Multi-Chip Module and PCB
- Computer interface and system integration with industrial standards

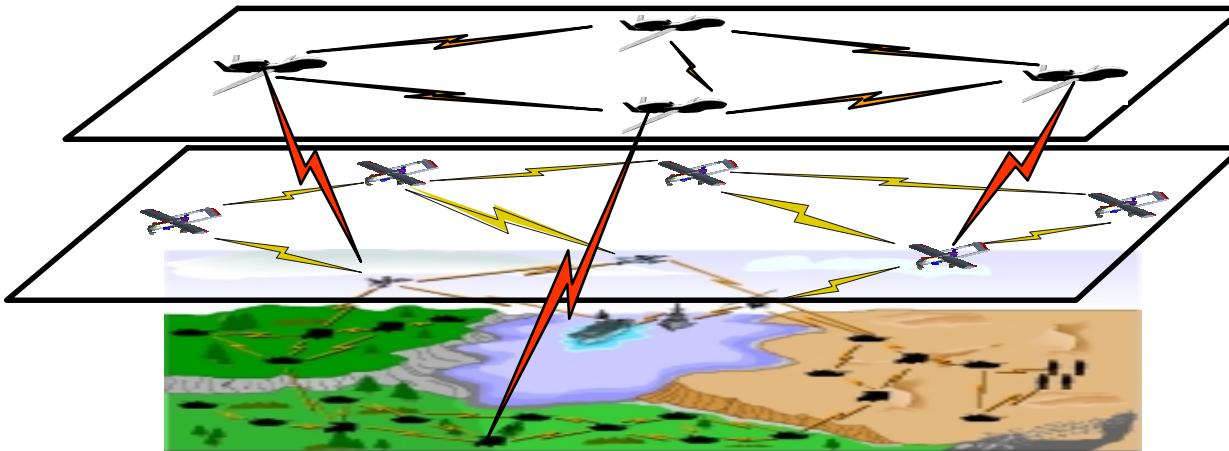


III-V HBTs Transferred
to Surrogate Substrate



InP HBT/ Optical Component Integration

- Developed high-performance dynamic networking architecture, protocols, and systems for DARPA
 - Adaptive C4ISR Network (ACN): DARPA ATO
 - Next Generation Internet (NGI): DARPA IPTO



- Dynamic multi-tier ad hoc routing
- Scalable QoS provisioning
- 3-D ACN network simulation
- Prototype development and demonstration

- Has extensive knowledge in:
 - High-speed switching algorithms for ATM and WDM.
 - Advanced internet and tactical traffic dynamics modeling
 - Self-similar traffic models
 - Inter-domain IP routing and its interaction with wavelength routing